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Applicants:	K. HORIKOSHI, et al.
Application No.:	09/988,585
Filed:	November 2, 2001
For:	THIN-FILM TRANSISTOR AND METHOD OF MANUFACTURING THE SAME
Art Unit:	2811
Examiner:	T. F. Tran

DECLARATION UNDER 37 CFR 1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Kazuhiko HORIKOSHI, a Japanese citizen residing in Yokohama, Japan, declare:

That I am the first-named inventor of the joint inventorship of the above-identified application and I am familiar with the present invention including the disclosed contents as well as the prosecution history of said application;

That I graduated in March 1987 from Hokkaido University, in Japan, Faculty of Science, and I have also completed a Master's Program in Science and Engineering, Course in Chemistry, in March 1990, at the University of Tsukuba, in Japan;

That on April 1990 I began my employment as an engineer at the Production Engineering Research Laboratory at Hitachi, Ltd. and that I have been engaged

during my tenure there in thin-film formation/technology which has particular application to thin film transistor technology;

That my work experience at Hitachi, Ltd., which continues to the present, mainly concerned thin film formation technology such as in connection with inorganic insulation films, dielectric films and so forth and included (i) investigating the characteristics and properties thereof including the physical properties of the same and (ii) the development of advancements in that area of technology including that disclosed in the above-identified application and also that published in (a) Ferroelectrics, Vol. 225, pp 163-170, 1999, (b) Proceedings in the Journal of Ferroelectrics, 1998, pp 940-943 and (c) Japanese Patent No. 3419695;

That I have read and understand the contents of Japanese Published Application JP 08-195494 (henceforth referred to as Abe et al.), presently cited by the Examiner against the above-identified application, as well as the contents of U.S. Patent 6,025,630 (henceforth referred to Yamazaki et al.), which document is of record and was earlier cited against said application.

That my background including formal education and experience working in this area of technology is evidence of my competency regarding the matters discussed in this declaration;

That the "glass substrate" of the present invention is a structure whose physical properties are different from that employed by either Abe et al. or Yamazaki et al., therefore, the thin-film transistor according to the present invention is characterized by a different structure from that taught by either Abe et al. or Yamazaki et al. (it will be shown hereinbelow that the glass substrate employed by Abe et al. as

well as Yamazaki et al. had to be a structure having different physical properties from that of the present invention so as to assure a low compaction [low shrinkage] when it is used at the relatively higher temperatures in the formation of the insulating film(s), in both Abe et al. and Yamazaki, et al.);

That a glass substrate whose structure is characterized by the physical properties set forth in claims 1 and 9 cannot be used in a scheme such as taught by either Abe et al. or Yamazaki et al. since this would lead to a defective TFT (this is because the compaction rate (heat shrinkage) of a glass substrate having the physical property set forth in claims 1 and 9 would be too great if exposed to processing conditions used by Abe et al. or Yamazaki et al. in the formation of the gate oxide insulating film(s);

That to prove that the "glass substrate" of the present invention is a different structure than that required by Abe et al. as well as Yamazaki et al. in connection with their processing scheme for achieving a TFT and, therefore, also show that a TFT according to the present invention is structured differently from that disclosed by Abe et al. as well as Yamazaki et al., I conducted four (4) experiments as detailed in part I, below (the results of which are discussed in parts II and III):

I. EXPERIMENTS

Experiment No. 1. This experiment, which is directed to the manufacture of the TFT (thin-film transistor) based on the example first embodiment of the present application, was undertaken as follows:

a. An amorphous silicon film was formed on a glass substrate (a grown glass substrate under the trade name of Corning 7059 which was not subjected to any pre-heating process was used as

the glass substrate in this experiment as well as in Experiments 2 and 3).

b. A polycrystalline silicon layer was subsequently formed by laser annealing.

c. A pattern was formed on the polycrystalline silicon layer using a normal photo-process (In this phase, alignment marks were formed for aligning a mask and distances between alignment marks in both the x-direction and y-direction were measured and are referred to as distances (X1, Y1).

d. The surface of the polycrystalline silicon layer on which a pattern was formed was then oxidized (the process included the formation of an SiO_2 film having a thickness of 10 nm and formed in an atmosphere including ozone at a temperature of 450° C for thirty minutes).

e. A SiO_2 layer having a thickness of 90nm was formed by a plasma-CVD method.

f. A gate region was then formed, which was then used as a mask for implanting impurity ions into the underlying polycrystalline layer to form the source and drain regions.

g. A RTA (Rapid Thermal Annealing) process for activating impurities was performed, and then a heating process was performed inside a furnace (in a nitrogen atmosphere at 450° C for one hour).

h. An interlaminar insulating layer and the electrodes were formed to complete the TFT (the interlaminar insulating layer relates to insulating layer 10 in Fig. 1 of the drawings).

Steps (d) and (e) are discussed in the second paragraph on page 9 of the original specification and regarding the silicon oxide film thickness of 10nm, this is consistent with the discussion related to Fig. 3 of the drawings in which the film thickness of the first silicon oxide layer 6a should be 4nm or larger in order to assure a flat-band voltage, which leads to more desirable transistor characteristics.

Experiment No. 2. Yamazaki et al.'s oxide film forming process was employed instead in the formation of the gate insulating film in the TFT manufacturing scheme according to the above Experiment No. 1 to show that a glass substrate whose structure is characterized by a physical property as that of the present invention cannot be used in the manufacture of a TFT where the gate insulating film is formed in accordance with the process employed in Yamazaki et al. Regarding this, the following experimental procedures were effected: in place of steps (d) – (e) in the above manufacturing Experiment 1, the oxide film forming process employed by Yamazaki et al. was used instead, in which: an oxide (SiO_2) layer having a thickness of 100nm was formed by plasma CVD under a heat condition of 300° C and an atmospheric pressure of 5Pa, using $TEOS/O_2$ as the material gas; thereafter, the SiO_2 layer was subjected to a heating process in argon (Ar) atmosphere for 1 hour, at a temperature of 550° C.

Experiment No. 3. Abe et al.'s oxide film forming process was employed instead in the formation of the gate insulating film in the TFT manufacturing scheme according to the above Experiment No. 1 to show that a glass substrate whose structure is characterized by a physical property as that of the present invention cannot be used in the manufacture of a TFT where the gate insulating film is formed in accordance with the process employed in Abe et al. In place of steps (d) – (e) in the above Experiment No. 1, the oxide film forming process used by Abe et al. in the formation of the gate insulating film was implemented. Namely, after processing in an atmosphere containing ozone under a temperature condition of 600° C for 30 minutes, a SiO_2 layer having a thickness of 90nm was formed under a temperature condition of 300° C in an atmosphere pressure of 5Pa, using $TEOS/O_2$ as the material gas.

Experiment No. 4. In this procedure, the above Experiment No. 1 was modified so that in place of the glass substrate which was not subjected to any prior heating process, a commercially available Corning 7059 glass (a glass substrate that was previously subjected to heat treatment by the manufacture), was instead used. Moreover, in place of the procedures according to steps (d) – (e) in the Experiment 1 above, the oxide film forming process (for forming the gate insulating film) of Yamazaki et al. was performed, namely, a SiO_2 layer of 100 nm thickness was formed by plasma CVD under a temperature condition of 300° C and atmospheric pressure of 5Pa, and using $TEOS/O_2$ as a material gas and, thereafter, the SiO_2 layer was subjected to a heating process in an atmosphere of Ar for one hour, at a temperature of 550° C, consistent with the above Experiment No. 2.

II. MEASURING CHARACTERISTIC VALUES

At the end of each of the above performed experimental procedures, Nos. 1-4, the following characteristics which directly affect the reliability/effectiveness of the produced TFT were considered:

(i) TFT characteristics: Upon completion of step (h) in each of the above four experiments, a representative characteristic V_{FB} (flatband voltage) was measured.

(ii) Glass compaction: After completion of step (h) in each of the four experimental procedures performed, a new measurement was made of the distances between the alignment marks in both the x-direction and y-direction. The distances between the alignment marks measured at the end of each of the above four experiments were set as distances X2, Y2. Then by comparing the distances measured between the alignment marks following step (h) in the experimental procedure with that measured in step (c), which is prior to the formation of the oxide films according to steps (d) – (e), the glass compaction which relates to heat shrinkage of glass was calculated. In these experimental procedures, glass compaction is defined as (X1-X2)/X1, (Y1-Y2)/Y1. (In these experiments, distances between alignment marks were measured by a precision automatic 2-dimensional measuring device SMIC-300, manufactured by SOKKIA.)

The results of these measured characteristics, related to the above-performed experimental procedures, are given in **Appendix A**, attached hereto. The chart in Appendix A gives the measured characteristics associated with each of the above performed Experiments 1-4, in which the column labeled *Process Condition* refers to

the temperature conditions on the poly-Si film layer in connection with the formation of the insulating films such as referred to in steps (d) – (e). Related discussions in the present specification as well as in Yamazaki et al. and Abe et al., as it relates to the temperature conditions with regard to Experiments 1-4, is also noted in that column. The column with the heading *glass substrate* is self-understood and the heading *Characteristics* is divided into two columns, including a column for the glass compaction measurements as well as a column for the flatband voltage (V_{FB}).

III. SUMMARY OF EXPERIMENTAL RESULTS

According to Experiment I, directed to the present invention, the glass substrate used was not subjected to a heating process (at the manufacturer) prior to its use in the manufacturing process for a TFT, that is, the glass substrate employed is one which has "a physical property such that its compaction is 30ppm or higher...," as defined in claims 1 and 9. When a TFT is manufactured using such a glass substrate in a process involving temperature levels reaching 450° C such as in connection with the formation of the SiO_2 oxide film(s), the compaction of the glass substrate was measured at about 8-10ppm, which is within the acceptable range. This allows for the formation of additional layered patterns to be formed thereon such as would be employed in connection with the manufacture of LCDs. That is, since the glass compaction is within the acceptable range, mask alignment of various patterns such as a wiring pattern, pixel pattern, color filter pattern, and so forth, can be effected with regard to a later process that will be within the design permissible values. That is, a TFT manufacturing process employing a heating history that is not raised beyond

about 450° C, for example, affords the use of a glass substrate whose structure is defined by a physical property as that referred to above, consistent with that set forth in the claims.

Generally, in the manufacturing process of a liquid crystal display panel using TFT technology, it is common knowledge that in the construction of a process design, deformation (e.g., heat shrinkage or compaction) of a glass substrate to be used should be restrained to 10-20ppm, which is measured in terms of the alignment accuracy of the pattern mask. This is explained in *A Handbook on Liquid Crystal Display Panel Manufacturing Technique*, p 193, 1992, published by Science Forum, a copy of which is attached hereto [a copy of the same was also submitted earlier as an attachment to the Amendment of December 19, 2002].

As is also shown in Appendix A, the manufactured TFT according to the process in Experiment No. 1 was achieved with excellent TFT characteristics noting that its flatband voltage is from 0 to -0.2V.

On the other hand, using the results of these experiments, if a TFT is manufactured using the same type of glass substrate as in Experiment No. 1 but, however, under the process conditions of Yamazaki, et al. (Experiment No. 2) and Abe et al. (Experiment No. 3), in which the silicon oxide film forming processes directed thereto occur at a process temperature of 550° C and 600° C, respectively, the glass substrate shows an excessively high heat compaction of 60ppm, using Yamazaki et al.'s silicon oxide film process, and 90ppm, using Abe et al.'s silicon oxide film forming process. These values are way outside the permissible deformation amounts for glass substrates. This is evidenced by the fact that it was

impossible to achieve an accurate alignment of a pattern mask and, as a result, the TFT could not be reliably manufactured.

In the Experiment No. 4, which involved the same process as that according to Experiment No. 2 (which used the process for the formation of the SiO_2 film according to Yamazaki et al.), I made a substitution in the glass substrate employed. Namely, according to Experiment No. 4, rather than employing a previously unheated grown glass substrate (i.e., an unannealed glass substrate), an annealed glass substrate was instead employed (i.e., a glass substrate that was involved in a heating process after it was grown). Namely, the grown glass substrate had been subjected to a heating process at a temperature of at least 600° C, at the glass manufacturer. From the experimental results obtained in Appendix A, it is noted that the compaction rate of the annealed substrate, according to Experiment No. 4, was so restrained that it could very safely withstand a normal (i.e., conventional) TFT manufacturing process (e.g., a process involving temperatures of 600° C or lower) without any problem.

Other than the type of glass substrate employed, there were no additional differences between the process involved in Experiment No. 2 and that involved in Experiment No. 4. However, unlike Experiment No. 2, the process according to Experiment No. 4 obtained very favorable results in terms of the glass compaction and the flatband voltage, as shown in Appendix A. Even though the process temperatures in Yamazaki et al. led to an excessive deformation amount when the glass substrate employed had a structure of a physical property consistent with that defined in claim 1 or claim 9 of the present invention (see Experiments Nos. 2 and 3), such excessive deformation did not occur in Experiment No. 4. This is because the

glass substrate used in Experiment No. 4 was already annealed beforehand, thereby raising its strain point. Subjecting such an annealed glass substrate to process conditions at such high temperatures (for forming oxide films) as that used in Experiment Nos. 2 or 3 would not lead to a heat shrinkage rate (compaction) that is outside the acceptable rate. This is confirmed from the results achieved with regard to Experiment No. 4 in which the glass compaction was determined to be at a very acceptable rate of 6ppm and, it is also noted, the resulting TFT characteristics show a flatband voltage of about 0V, which is considered excellent.

From the results achieved in Experiment No. 4, it is apparent that a glass substrate having physical properties as that according to the present invention does achieve satisfactory results when employed in a manufacturing scheme under heat processing conditions of Experiment No. 1, which is based on that employed to achieve the TFT of the present invention. For manufacturing schemes such as in Yamazaki et al. or, in Abe et al., which used much higher temperature processing conditions in the formation of the silicon oxide film, as noted in Experiment Nos. 2 and 3, a glass substrate that has not undergone an annealing process beforehand could not be used, as evidenced by the results achieved. This conclusion is also supported by the fact that favorable results were achieved in Experiment No. 4, which implemented Yamazaki et al.'s higher temperature processing conditions for the formation of the silicon oxide film of a TFT manufacturing scheme using a glass substrate that has already undergone a heat treatment, i.e., using an annealed glass substrate, the characteristics of which leads to a much higher strain point than that of a glass substrate that has not undergone a pre-annealing process. That is, at such

high temperatures as that employed by Yamazaki et al. and Abe et al., in connection with the formation of the SiO_2 films, the glass substrate must be such that it has a physical property in which at a temperature as high as 600° C, the glass compaction must be substantially lower than the 30ppm or higher (at that temperature) in order to achieve favorable results. Consistent with the experimental results in Appendix A, in order to achieve acceptable heat compaction rates and TFT characteristics, the glass substrate employed in Yamazaki et al.'s and Abe et al.'s process must necessarily be that of an annealed glass substrate. With regard to Abe et al.'s TFT manufacturing scheme which employed even higher processing temperatures than that of Yamazaki et al. in the formation of the oxide films, e.g., a processing temperature of 600° C, it is even more paramount to use an annealed glass substrate whose constraint point is such that it achieves an acceptable compaction even at 600° C. It is submitted, consistent with the results in Appendix A, a glass substrate whose structure is defined by a physical property as that according to the present invention, which was used with satisfactory results in Experiment No. 1, cannot be employed in the TFT process according to Yamazaki et al. and Abe et al.

I declare, therefore, that based on the above-described experimental results, in order to be able to achieve a favorable outcome involving the manufacture of the TFT according to both Abe et al and Yamazaki et al., it is necessary to use as a glass substrate one that has already been subjected to a heating process in order to lower the heat shrinkage rate (compaction) at temperatures as high as 600° C when employed in a later heating process such as in the formation of gate oxide insulating film(s) for TFTs. (To have a lower heat shrinkage rate (compaction) in a later heat

process having temperatures as high as 600° C requires that the annealed glass substrate have a higher strain point than that of a glass that had not undergone a preheating process. Since a strain point is associated with temperatures and the higher the strain point the higher the temperature at which the heat compaction rate starts to increase significantly, an annealed glass is therefore more desirable when the process involves temperatures as high as that used by Yamazaki et al. and Abe et al.)

I declare that based on the evidence presented herein, the TFT structure of Abe et al. as well as Yamazaki et al. is different from that of the present invention at least in terms of the physical properties of the glass substrate structure employed.

I declare that because in processes in which a glass substrate is heated with temperatures as high as that called for by Abe et al. and Yamazaki et al. can be avoided with regard to achieving the present invention, the present invention has a great advantage over that of Yamazaki et al. and Abe et al. in that the process of manufacture of the TFT can be simplified and the cost of manufacturing the TFT can be significantly lowered.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Application No.: 09/988,585

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March 3, 2004

Date

Kazuhiko Horikoshi

Kazuhiko HORIKOSHI

Attachments: Appendix A
A Handbook on Liquid Crystal Display Panel Manufacturing Technique, p 193